













of Electronics Engineering, (2010), pp. 197-203.

- [10] K. Nagalexmi , B. Vasu Naik , “Design and Implementation Floating Point Multiplier Design using Combined Booth and Dadda Algorithms”, International journal of VLSI systems and Communication Systems, ISSN 2322-0929 Vol.03, Issue.04, July-2015, Pages:0496-0499
- [11] V.Sudhakar, N.S.Murthy, L.Anjaneyulu, “Area Efficient Pipelined Architecture for Realization of FIR filter using Distributed Arithmetic”, IPCSIT Press Vol 31, Singapore.
- [12] Anshika Rajolia, Maninder Kaur, “Finite Impulse Response(FIR) Filter Design Using Canonic Signed Digit (CSD)”, IJSR, Vol-2 Issue 7, July 2013.
- [13] Basant Kumar Mohanty , Pramod Kumar Meher, “A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 24, No. 2, February 2016.
- [14] Aarti Sharma & Sanjay Kumar, “VLSI Implementation of Pipelined FIR Filter”, International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering Vol. 1, Issue 5, August 2013.
- [15] Thamizharasan V & Parthipan V, “An Efficient VLSI Architecture for FIR Filter using Computation Sharing Multiplier”, International Journal of Computer Applications (0975-8887) Volume 54- No.14, September 2012.
- [16] Deepa Yagain & Dr. Vijaya Krishna A, “FIR Filter Design based on Retiming & Automation using VLSI Design Metrics”, 2013 International Conference on Technology, Informatics, Management, Engineering & Environment.
- [17] Kam Hoi Cheng & Satraj Sahni, “VLSI Architectures for the Finite Impulse Response Filter”, IEEE Journal on Selected Areas in Communications, Vol. sac-4, No.1, January 1986
- [18] Prathibha P Nair, Tintu Mary John, “Optimized FIR filter using distributed parallel architectures for audio application”, International Journal of Computer Technology & Applications, Vol. 8 (3), June 2017
- [19] ”Design of FIR Digital Filters with CSD Coefficients Having Power-of-Two DC Gain and Their FPGA Implementation for Minimum Critical Path”, Researchgate Article, August 2001
- [20] Sonal Gupta, Umashankar Kurmi “A Review - Design of Area and Power Efficient Digital FIR Filter Based On Faithfully Rounded Truncated 12-Bit Constant”, International Journal of Computer Applications (0975 – 8887) Volume 149 – No.6, September 2016.