Engineering World
Open Access Journal
ISSN: 2692-5079

High-Efficiency Doherty Power Amplifier Based on an Asymmetric Structure

Bin Wang, Jiang Teng, Xin Zhang, Dong Su and Wei Luo

***Abstract*—**This study presents a Doherty power amplifier (DPA) based on an asymmetric structure using an uneven power divider and different power amplifier(PA) transistors between main and auxiliary PAs, which not only expands the power back-off level but also achieves a high efficiency. After providing an analysis of the fundamental theory, a design guide for the proposed DPA is presented. For verification, the conventional and proposed DPAs are designed and compared. Using test instruments from Agilent, the proposed DPA exhibits comparably better performances than the conventional DPA, such as a high power-added efficiency of 44%, a power back-off level as high as 7dB, and a power gain of 13dB at the output power of 42dBm.

***Keywords*—**Power amplifier, Doherty, high efficiency, asymmetric structure, power back-up

I. INTRODUCTION

POWER amplifiers (PAs) used in modern wireless communication systems are required to maintain high efficiency at power back-off level from the peak output power. Many classical techniques that enhance the efficiency with high power back-off level have been reported in previous studies. Among these techniques, the Doherty power amplifier (DPA) is mentioned repeatedly due to its structural simplicity and well performance.The DPA was first proposed by William Doherty in 1936 [1]. The basic concept of the DPA is the changes in the output load impedance of the main and auxiliary PAs. The class-AB PA is used as the main amplifier stage. The conventional DPA has an even input power and the same PA transistors for the auxiliary and main PAs. This symmetric structure yields high efficiency at 6dB power back-off level theoretically [2], [3].

However, 6dB power back-off level cannot meet the requirements of the signal with high peak-to-average power ratio (PAPR). Thus, this study aims to provide a DPA based on an asymmetric structure to solve this problem. A high peak output power benefits the power back-off level [4]. Generally, different PA transistors have different peak output powers, and the auxiliary PA needs higher peak output power than the main PA. Alternatively, an uneven power divider can drive more power to the auxiliary PA to compensate the low power gain of auxiliary PA and expand the power back-off level. With the asymmetric structure, the DPA can obtain more than 6dB power back-off level theoretically [5].

This study presents a DPA based on an asymmetric structure using an uneven power divider and different PA transistors. The class-C auxiliary PA acquires more input power, and its peak output power is greater than the main PA. Meanwhile, the bias voltages are adjusted to obtain better gain, efficiency and power back-off level [6]. For verification, the conventional and proposed DPAs based on an asymmetric structure are designed and implemented for a 2.11GHz-2.17GHz band, the bandwidth is 70MHz, which is a quite excellent bandwidth for communication systems. In some researches [7], [8], the authors throw a way by compensating the parasitic elements of transistors to expand the bandwidth of the power amplifier effectively.

II. DOHERTY CONCEPT

The DPA did not attract sufficient attention when it was first proposed in 1936. However, the efficiency of this technology has been remarkably enhanced in recent years. The structure of the conventional DPA is shown in Fig. 1. The DPA consists of a power divider, main PA, auxiliary PA, and power combination network. Besides, coupler [9] and harmonic suppressed wilkinson power divider [10] in some designs are selected to improve the bandwidth and efficiency of the DPA. The main PA works in class-AB or -B bias condition, whereas the auxiliary PA works in class-C bias condition.

As shown in Fig. 1, the input signal is divided by the power divider to distribute to the two PAs and amplified with high efficiency by the load modulation. According to the active load-pull theory [11], [12], the two PAs can be regarded as the current sources. The equivalent circuit is shown in Fig. 2, and two formulas can be derived.

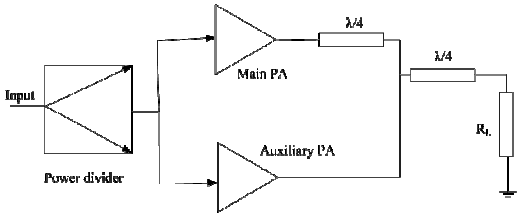


Fig. 1 Structure of the conventional DPA.

This work was supported in part by the National Natural Science Foundation of China under Grant No.41606203.

The authors are all with the College of Electronic Engineering, Chongqing University of Posts and Telecommunications, Chongqing, 400065, China.

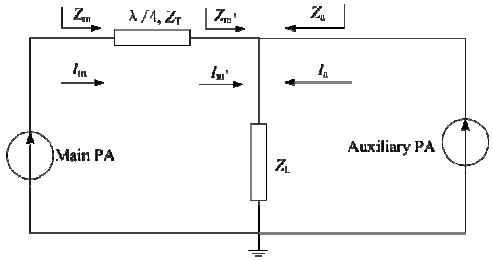


Fig. 2 Equivalent circuit of the DPA.

$$Z_{\mathrm{m}}=\begin{cases}\dfrac{Z_T^2}{Z_L} & 0<V_{in}\le\dfrac{V_{\max}}{2}\\ \dfrac{Z_T^2}{Z_L(1+\alpha)} & \dfrac{V_{\max}}{2}<V_{in}\le V_{\max}\end{cases}\tag{1}$$

$$Z_{\mathrm{a}}=\begin{cases}\infty & 0<V_{in}\le\dfrac{V_{\max}}{2}\\ Z_L\left(1+\dfrac{1}{\alpha}\right) & \dfrac{V_{\max}}{2}<V_{in}\le V_{\max}\end{cases}\tag{2}$$

where V_{in} is the input voltage, $V_{\max}$ is the peak voltage, Z_m is load impedance of main amplifier, Z_L is load impedance of the DPA, usually Z_L is 50Ω, and α is power allocation factor, $\alpha=I_a/I_m$, $\alpha\in(0,1)$. The ideal characteristics of the voltage and current waveforms of a two-branch DPA for the entire range of the input signal is shown in Fig. 3.

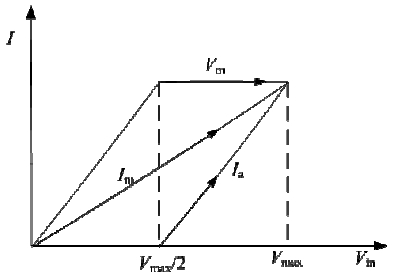


Fig. 3 Current and voltage characteristics of the DPA.

From Fig. 3 and (1) and (2), the DPA has three working categories, that is, low, medium, and high power level.

A. Low Power Levels

Only the main PA is on operating, the auxiliary PA is turned off. The linearity and efficiency of this region are based on class-AB operation before the main PA operates to its saturation point. Theoretically, when the main PA reaches its saturation point, the maximum efficiency of the DPA is achieved first time.

B. Medium Power Level

The auxiliary PA starts to operate while the main PA still operates as the current source. The load impedance of the main and auxiliary PAs are modulated, which results in the changes in load impedance of the main and auxiliary PAs.

C. High Power Level

At this region, main and auxiliary PAs are saturated and the maximum efficiency of DPA is achieved again.

The analysis of the concept of DPA shows that the DPA can achieve high efficiency within a certain power back-off level. This feature can make the DPA amplify the high PAPR signal with high efficiency. Theoretically, symmetric DPA that adopt two similar transistors can obtain 6dB power back-off level with high efficiency. By contrast, asymmetric DPA can achieve higher back-off level with a diverse designs [13]-[15].

Generally, the mainly method to build an asymmetric DPA is to use different PA transistors with an uneven power divider. The power back-off level can be expressed as below [16]:

$$\beta=20\lg\frac{P_m}{P_m+P_a}\tag{3}$$

Where β is the power back-off level, and P_m and P_a are the saturated output power of the main and auxiliary PAs, respectively. (3) indicates that if the ratio of saturated output power between the auxiliary and main PAs is 2:1, then the power back-off level is approximately 9 dB.

The efficiency of the symmetric and asymmetric DPAs are depicted in Fig. 4. Theoretically, both structures of the DPA can achieve a drain efficiency of 78.5% at the power back-off point and the peak output power when the main amplifier works in the class-B condition.

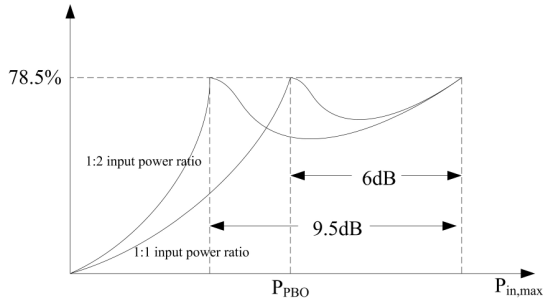


Fig. 4 Drain efficiency of symmetric and asymmetric DPAs.

III. Design of The Proposed Dpa

In this work, MRF8S21100H and MRF7S21080H transistors from NXP are used for the simulation and implementation. Theoretically, MRF7S21080H provides 49dBm (80W) output power at the 1dB compression point, whereas MRF8S21100H provides 51.5dBm (141W) output power at the 1dB compression point, the power ratio of the two transistors is approximately 1:2. All of the simulations are conducted using the ADS software from Agilent and account for additional losses of the structure bonds, as well as the coupling effect in EM simulation environment.The measured performances of the two DPAs are compared using test instruments from Agilent.

ISSN: 2692-5079

The two DPAs proposed in this study can cover a 2.11GHz-2.17GHz band, which is one of the downstream frequencies in LTE applications. The performance requirements are listed as below. The maximum output power in the simulation is over 53dBm, and the gain plainness is lower than 1dB. For the symmetric DPA, the output power back-off level should be greater than 6dB; whereas for the asymmetric DPA, the output power back-off level should be greater than 9dB. Both DPAs are required to achieve high gain and high efficiency. DPA design has three steps, namely, power divider design, main and auxiliary PAs design, and circuit optimization.

In this study, firstly, a Wilkinson power divider is selected in both DPAs. The power divider of the symmetric DPA needs 1:1 power allocation ration, whereas that of the asymmetric DPA needs 1:2 because the auxiliary PA needs more input power to increase the power back-off level.

Second, MRF8S21100H and MRF7S21080H transistors are selected as the auxiliary and main PAs in the asymmetric design, respectively. A stability analysis is necessary prior to the PA design, and the stability of MRF8S21100H and MRF7S21080H is validated using the ADS software. Then, an important part of the main and auxiliary PA design is to determine the load/source impedance of the selected transistors over the desired bandwidth. Usually, the data sheet of the transistor provides reference impedance values. However, through the combination of the large-signal model of the selected transistors and the load/source pull simulation in the ADS software, which can obtain the optimal values, is adopted in this study. Input and output matching networks are designed after the load/source impedance have been determined. According to the concept of the asymmetric DPA, the matching network of the main amplifier needs to transform the optimum impedance extracted from the load-pull simulation to 50Ω. And through repeated debugging and optimization the output matching network of the auxiliary PA needs to transform the impedance from the load-pull simulation to 40Ω, which can obtain the optimal results. Then, a quarter-wavelength microstrip line is chosen as the bias circuit for the two DPAs. Besides, optimizing the performance after designing the main and auxiliary PAs is necessary.

Finally, the circuits are combined and the performances of the DPA are optimized. Considerable modulation is needed to achieve the best performance in this step, and the final circuit of asymmetric DPA is shown in Fig. 5.

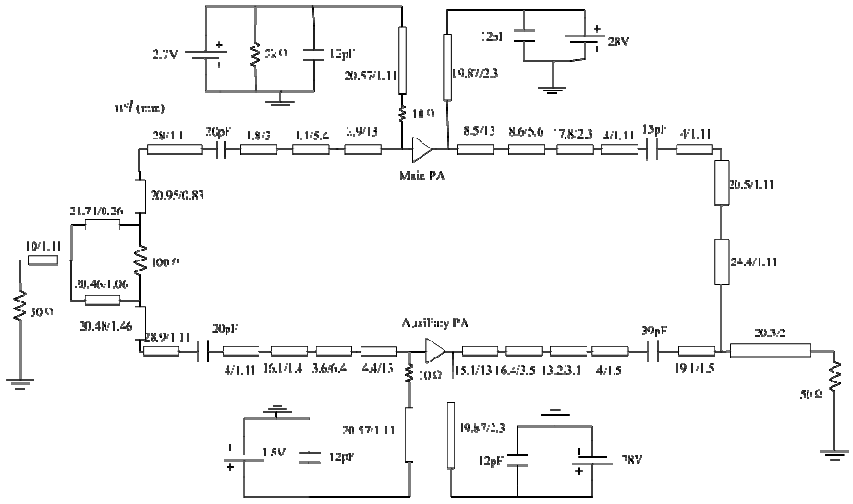


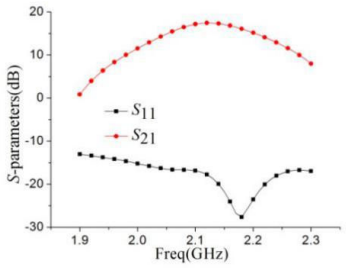
Fig. 5 Final circuit of asymmetric DPA

The steps of the symmetric DPA design are same as the asymmetric DPA design. However, its main amplifier transistor is MRF8S21100H. Matching networks of the main and auxiliary PAs need to transform the impedance from load-pull or source-pull simulation to 50Ω. The simulated results of the two DPAs at the end of the simulation are shown in Fig. 6.

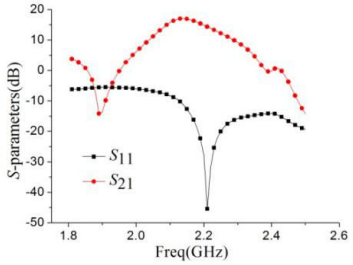
In Fig. 6(a) and 6(b), simulated S_{11} of the two DPAs are lower than −20dB in the 2.11GHz-2.17GHz band. These parameters ensure that the echo is sufficiently small. The gain of the two DPAs are around 17dB, which implies that the gain of the symmetric and asymmetric DPAs are the same.

In the large-signal simulation, the PAE and back-off power level are the most important parameters in DPA design. As shown in Fig. 6(c), the symmetric DPA yields 46% PAE at the 7dB output power back-off, which is a commendable result. However, the asymmetric DPA remarkably achieves the 9dB power back-off level, and its PAE is higher than 44% at the 9dB power back-off point. Meanwhile, a high power back-off level can be acquired by adjusting the bias voltages feasibly.

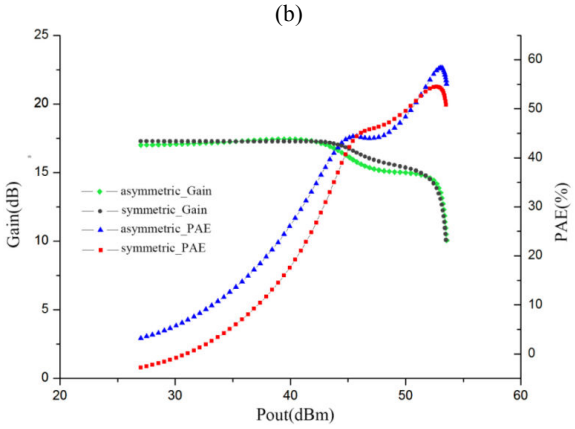
ISSN: 2692-5079



(a)



(b)

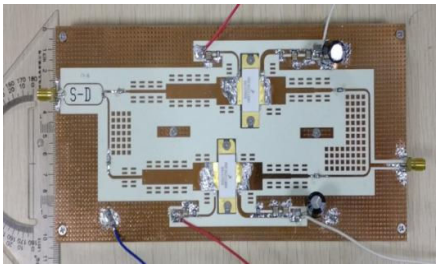


(c)

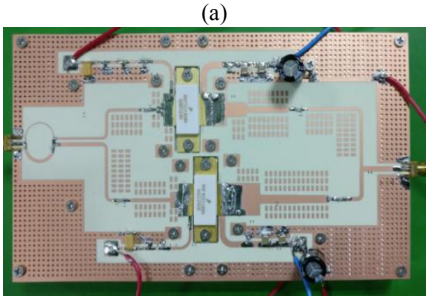
Fig. 6 Simulated results of two DPAs
(a) S-parameters of symmetric DPA
(b) S-parameters of asymmetric DPA
(c) Gain and PAE of two DPAs

IV. Experimental Results

The two DPAs are fabricated on the Rogers-4350B substrate with cooper mentalization (Rogers-4350B with ε_r=3.66, substrate H=0.508mm, and mental thickness t=0.035mm), as shown in Fig. 7. In this section, the experimental results of the two DPAs are compared. The bias voltages for the main PA of the asymmetric DPA are V_{gs}=2.9V and V_{ds}=28V , and that for the main PA of the symmetric DPA are V_{gs}=3.1V and V_{ds}=28V. The difference in V_{gs} is due to the transistor difference. The bias voltages for the two designs of the auxiliary PAs are V_{gs}=1.2V and V_{ds}=28V. A 10Ω resistance is added between the input matching network and the gate bias circuit in both designs to prevent the circuit from producing low-frequency self-excitation.



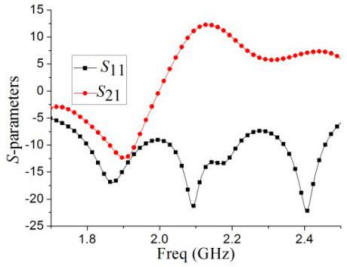
(a)



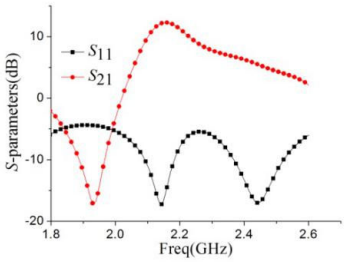
(b)

Fig. 7. Photographs of two DPAs
(a) symmetric, (b) asymmetric

Fig. 8(a) and 8(b) show the measured S-parameters of the two DPAs. The S-parameter test was conducted using the vector network analyzer N5242A from Agilent. As shown in Fig. 8(a), the S-parameters of the symmetric DPA meet the requirements, with S_{11} lower than −15dB and S_{21} higher than 12dB in the 2.11GHz-2.17GHz band. The measured S-parameters of the asymmetric DPA also meet the requirements, with S_{11} lower than −17dB and S_{21} approximately 13dB in the working frequency band.



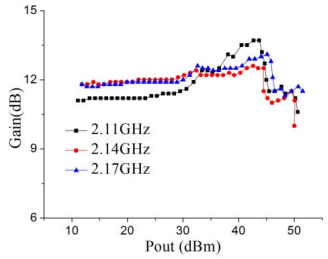
(a)



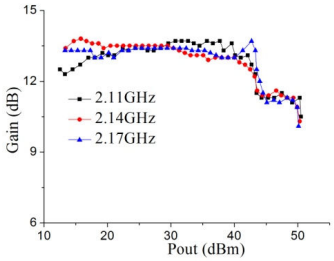
(b)

Fig. 8 Measured S-parameters of two DPAs
(a) Symmetric
(b) Asymmetric

The measured results of gain and PAE are shown in Fig. 9 and Fig. 10. Measured gain and PAE as a function of the output power for the two DPAs. The input signal are three single tone continuous waves at 2.11GHz, 2.14GHz, 2.17GHz, respectively. As can be seen in Fig. 9, the gain is approximately 12dB of the symmetric DPA at the 2.14GHz and 2.17GHz. Whereas, the gain at 2.11GHz is not preferable. In the proposed asymmetric DPA, 13dB gain is obtained that is higher than symmetric one. And the gain of asymmetric DPA in working frequency band is more steady than symmetric DPA.



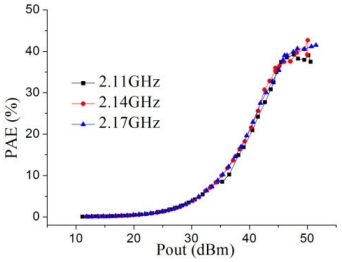
(a)



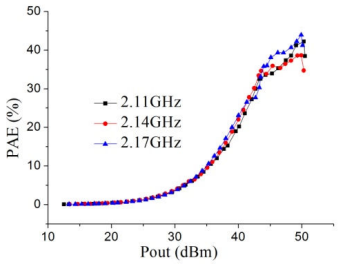
(b)

Fig. 9 Measured Gain of two DPAs
symmetric, (b) asymmetric.

The measured PAE of two DPAs are depicted in Fig. 10. Fig. 10(a) shows the maximum PAE of the symmetric PA is approximately 42%, which obtains 5dB power back-off(PBO) level and PAE_{5dB}=36%. Meanwhile, it can be seen that about 44% maximum PAE and 7dB power back-off level are obtained as shown in Fig. 10(b). It can be found that asymmetric DPA obtains larger power back-off level than symmetric one. Obviously, by large-signal measurements at 2.11GHz, 2.14GHz, 2.17GHz respectively, the two DPAs have well performances in working frequency band.

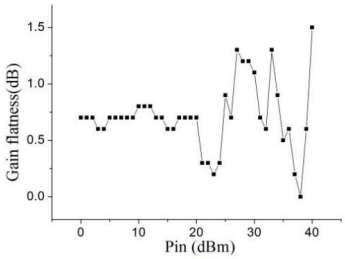


(a)

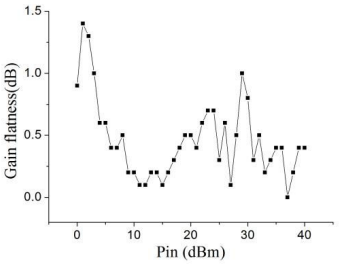


(b)

Fig. 10 Measured PAE of two DPAs
(a) symmetric, (b) asymmetric.



(a)



(b)

Fig. 11 Measured Gain flatness of two DPAs
(a) symmetric, (b) asymmetric

The measured gain flatness are depicted in Fig. 11. The gain flatness of symmetric and asymmetric DPAs are almost lower than 1dB, that means that the two DPAs have an excellent gain flatness. Overall, the measured results of the two DPAs show that the two DPAs can be used for base stations.

Table I. Performance comparisons with some previous studies

Ref.	Freq (GHz)	Gain (dB)	PBO (dB)	PAE_{OBO} (%)	Pout (dBm)
[17]	1.85	12	6	23.4	P_{sat}<30
[18]	1.88	23	6	42	33.5 @P1dB
[19]	2.14	16.6	6.5	57.8	36.9 @Paverage
[20]	2.14	13	9	50	46 @Psat
Symmetric	2.14	12	5	36	50 @Psat
Asymmetric		13.5	7	35	51 @Psat

As shown in Table I, the proposed asymmetric DPA exhibits a competitive performance compared with those of other works. The frequency of the two DPAs in this study are similar to those of the references. However, the power back-off level in Refs [17] and [18] are lower than the 7dB dB which is obtained for the asymmetric DPA in this study. Furthermore, the PAE in Ref [17] is lower than the symmetric and asymmetric DPAs designed in this study. Notably, compared with the GaN HEMTs used in Refs [19] and [20], the MOSFETs used in this work are more economical but have comparable performances.

V. CONCLUSION

An asymmetric DPA with enhanced back-off efficiency and expanded power back-off level is fabricated and measured by the simple steps of setting an uneven power divider, selecting different PA transistors, and optimizing the matching networks. Meanwhile, a symmetric DPA is designed using the same transistor for the purpose of proving the concept of the DPA and comparing its performances with the asymmetric DPA. The measured results show that the output power of the symmetric and asymmetric DPAs are nearly the same. The power-added efficiency of the two DPAs are compared based on the power back-off level. The power back-off level of the asymmetric DPA reaches 7dB, which is 2dB greater than that of the symmetric DPA, and the PAE of two DPAs in the back-off level are nearly the same. Finally, the asymmetric DPA is proven to achieve a wider back-off power level than the symmetric DPA by chosen an uneven power divider and selecting different transistors.

REFERENCES

[1] Doherty W H. A new high efficiency power amplifier for modulated waves[J]. The Bell System Technical Journal. 1936, 15(3): 469-475.
[2] Liu Q A, S B He, and W M Shi. Design of 3.5GHz linear high efficiency Doherty power amplifierwith pre-matching[C]. 2015 Asia Pacific Microwave Conference (APMC). 2015, 1-3, NanJing, China.
[3] Xia J, M Yang, Y Guo, and A Zhu. A Broadband High-Efficiency Doherty Power Amplifier With Integrated Compensating Reactance[J]. IEEE Transactions on Microwave Theory and Techniques. 2016, 64(7): 2014-2024.
[4] Giofre R, P Colantonio, F Giannini, and L Piazzon. New output combiner for Doherty amplifiers[J]. IEEE Microwave and Wireless Components Letters. 2013, 23(1): 31-33.
[5] Son J, I Kim, J Moon, J Lee and B. Kim. A highly efficient asymmetric Doherty Power Amplifier with a new output combining circuit[C]. 2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS 2011). 2011, 1-4 , Tel, Aviv.
[6] Alexander A, and L Jonathan. Improving efficiency, linearity and linearisability of an asymmetric doherty power amplifier by modulating the peaking Amplifier's supply voltage[C]. 2017 47th European Microwave Conference (EuMC). 2017, 464-467, Nuremberg, German.
[7] Ardekani M H M, Abiri H. A New Approach to Design Wide Band Power Amplifiers by Compensating Parasitic Elements of Transistors[J]. AEU - International Journal of Electronics and Communications. 2018, 92: 1-7
[8] Ardekani M H M, Abiri H. Corrigendum to “A new approach to design wide band power amplifiers by compensating parasitic elements of transistors”[J]. AEU - International Journal of Electronics and Communications. 2018, 93: 215-215.
[9] Piazzon L, Giofre R, Colantonio P, and Giannini F. A method for designing broadband doherty power amplifiers[J]. Progress In Electromagnetics Research. 2014, 145: 319-331.
[10] Hayati M, Roshani S. A broadband Doherty power amplifier with harmonic suppression[J]. AEUE - International Journal of Electronics and Communications. 2014, 68(5): 406-412.
[11] Cai Y, C Yu, S Li, and Y Liu. Modified Doherty power amplifier based on asymmetric load matching networks[C]. 2016 11th International Symposium on Antennas, Propagation and EM Theory (ISAPE). 2016 739-742, GuiLin, China.
[12] Kim B, J Kim, I Kim, and J Cha. The Doherty power amplifier[J]. IEEE Trans. Microwave Magazine. 2006, 7(5): 42-50.
[13] Qi T, and S He. Design of High Efficiency Doherty Power Amplifier Applying Power Controlling Technology with15dB Output Power Back-off[C]. 2017 47th European Microwave Conference(EuMC). 2017, 576-579, Nuremberg, German.
[14] Xia J, X Zhu, L Zhang, J Zhai, and Y Sun. High-efficiency GaN Doherty power amplifier for 100-MHz LTE-advanced application based on modified load modulation network[J]. IEEE Transactions on Microwave Theory and Techniques. 2013, 61(8): 2911-2921.
[15] Iwamoto M, A Williams, P F Chen, A G Metzger, L E Larson, and P M Asbeck. An extended Doherty amplifier with high efficiency over a wide power range[J]. IEEE Transactions on Microwave Theory and Techniques. 2001, 49(12): 2472-2479.
[16] Nghiem X A, and R Negra. A highly efficient wideband asymmetric Doherty power amplifier with 10 dB output power back-off[C]. 2013 European Microwave Conference. 2013, 271-274, Nuremberg, German.
[17] Cho Y, D Kang, J Kim, K Moon, B Park, and B Kim. Linear Doherty power amplifier with an enhanced back-off efficiency mode for handset applications[J]. IEEE Transactions on Microwave Theory and Techniques. 2014, 62(3): 567-578.
[18] Kang D, Y Cho, D Kim, B Park, J Kim, and B Kim. Impact of nonlinear Cbc on HBT Doherty power amplifiers[J]. IEEE Transaction on Microwave Theory and Techniques. 2013, 61(9): 3298-3307.
[19] Oh H, H Kang, H Lee, H Koo, M Kim, W Lee, W Lim, C S Park, K C Hwang, K Y Lee, and Y Yang. Doherty power amplifier based on the fundamental current ratio for asymmetric cells[J]. IEEE Transaction on Microwave Theory and Techniques. 2017, 65(11): 4190-4197.
[20] Lee Y S, M W Lee, and Y H Jeong. Unequal-cells-based GaN HEMT Doherty amplifier with an extended efficiency range[J]. IEEE Microwave and Wireless Components Letters. 2008, 18(8): 536-538.