Impact of Gate Insulation Material and Thickness on Pocket Implanted MOS Device

Muhibul Haque Bhuyan

***Abstract*—**This paper reports on the impact study with the variation of the gate insulation material and thickness on different models of pocket implanted sub-100 nm n-MOS device. The gate materials used here are silicon dioxide (SiO_2), aluminum silicate (Al_2SiO_5), silicon nitride (Si_3N_4), alumina (Al_2O_3), hafnium silicate ($HfSiO_4$), tantalum pentoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), and lanthanum oxide (La_2O_3) upon a p-type silicon substrate material. The gate insulation thickness was varied from 2.0 nm to 3.5 nm for a 50 nm channel length pocket implanted n-MOSFET. There are several models available for this device. We have studied and simulated threshold voltage model incorporating drain and substrate bias effects, surface potential, inversion layer charge, pinch-off voltage, effective electric field, inversion layer mobility, and subthreshold drain current models based on two linear symmetric pocket doping profiles. We have changed the values of the two parameters, viz. gate insulation material and thickness gradually fixing the other parameter at their typical values. Then we compared and analyzed the simulation results. This study would be helpful for the nano-scaled MOS device designers for various applications to predict the device behavior.

***Keywords*—**Linear symmetric pocket profile, pocket implanted n-MOS Device, model, impact of gate material, insulator thickness.

I. Introduction

THE long-channel conventional bulk MOS devices have homogeneous doping concentration and accordingly the threshold voltage model was derived for them [1]. However, as the channel length of such devices was downsized to deep-sub-micrometer or beyond the 100 nm regime, Short-Channel Effects (SCE) started to arise. For the short-channel bulk MOS devices, the SCE includes the threshold voltage reduction, augmented leakage current during off-state, and punch through the bulk [2]. The SCEs are witnessed due to the 2-D nature of the surface potential and higher electric fields along the device channel. To combat these effects, horizontal channel doping engineering exploiting halo/pocket implant near the source and drain regions was found very useful, and as such corresponding MOS models for various parameters were developed [3]-[7]. If the doping concentration becomes non-homogeneous along the channel then it experiences the opposite effect on the threshold voltage called the Reverse Short-Channel Effect (RSCE) [8] that can annul the SCE of the MOS device [9]. In several earlier works of pocket implanted MOSFET modeling, it was shown that those models are capable of describing the behavior of the pocket implanted MOSFET for the channel length up to 50 nm [10], [11]. Those models incorporated several shapes of pocket profiles, like linear [12], Gaussian [13], and hyperbolic cosine [14] profiles. It was shown that the linear profile also works very well taking less simulation time [12]. However, as the channel length goes down, we have to reduce the gate insulation thickness and increase the gate dielectric constant to avoid threshold voltage lowering further and hence to improve the device performance parameters. It has already been established that by increasing the dielectric strength that is using high-*k* dielectric materials or by decreasing the gate insulation layer thickness, we can improve the performances of the conventional and advanced MOS devices [15]-[19]. However, this study was not extended to the pocket implanted nano-scaled devices. Therefore, in this work, we have studied various models of the pocket implanted MOS devices by changing the gate insulation materials and gate insulation layer thickness and analyzed their impacts on the device performance in the nano-scaled regime.

M. H. Bhuyan is with the Department of Electrical and Electronic Engineering (EEE), Southeast University, 251/1 & 252 Tejgaon Industrial cum Commercial Area, Dhaka 1208, Bangladesh (phone: 88-01815-657346; e-mail: muhibulhb@gmail.com).

II. Pocket Doped MOS Device Structure

The pocket embedded n-MOS device construction is shown in Fig. 1. The presumed co-ordinate scheme is presented at the right-hand part of the device construction.

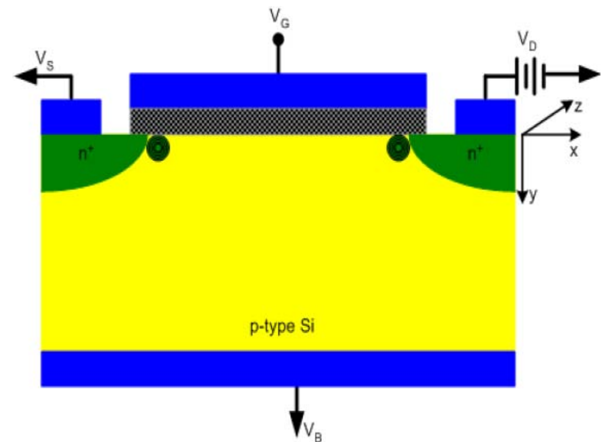

Fig. 1 Pocket embedded n-MOS construction with symmetric pockets both at the source and drain wings [21]

Table I shows all the device dimensions and parameters along with their symbols, values, and units used in this work. The device dimensions are measured according to the coordinate system of Fig. 1.

MOSFETs," IEEE Transactions on Electron Devices, vol. 44, pp. 627-633, Apr. 1997.
[3] B. Yu, H. Wang, O. Millic, Q. Xiang, W. Wang, J. X. An and M. R. Lin, "50 nm gate length CMOS transistor with super-halo: Design, process and reliability," IEEE IEDM Technical Digest, pp. 653-656, 1999.
[4] Y. S. Pang and J. R. Brews, "Models for subthreshold and above subthreshold currents in 0.1 m pocket n-MOSFETs for low voltage applications," IEEE Transactions on Electron Devices, vol. 49, no. 5, pp. 832-839, May 2002.
[5] M. K. Khanna, M. C. Thomas, R. S. Gupta and S. Haldar, "An analytical model for anomalous threshold voltage behavior of short-channel MOSFETs," Solid-State Electronics, vol. 41, pp. 1386-1388, 1997.
[6] H. Brut, A. Juge, and G. Ghibaudo, "Physical model of threshold voltage in silicon MOS transistors including reverse short channel effect," Electronics Letters, vol. 31, no. 5, pp. 410-12, March 1995.
[7] M. H. Bhuyan and Q. D. M. Khosru, "Low-Frequency Drain Current Flicker Noise Model for Pocket Implanted Nano Scale n-MOSFET," Proceedings of the IEEE and EDS sponsored Nano Materials and Device Conference (NMDC), 12-15 October 2010, CA, USA, pp. 295-299.
[8] M. H. Bhuyan and Q. D. M. Khosru, "An analytical surface potential model for pocket implanted sub-100 nm n-MOSFET," Proceedings of the 5th IEEE International Conference on Electrical and Computer Engineering, Dhaka, 20-22 December 2008, pp 442-446.
[9] M. H. Bhuyan and Q. D. M. Khosru, "Linear pocket profile based threshold voltage model for sub-100 nm n-MOSFET," International Journal of Electrical and Computer Engineering, vol. 5, no. 5, pp. 310-315, May 2010.
[10] M. H. Bhuyan, "Analytical modeling of the pocket implanted nanoscale n-MOSFET," PhD Thesis, Department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, Dhaka, Bangladesh, 2011.
[11] M. H. Bhuyan and Q. D. M. Khosru, "An analytical subthreshold drain current model for pocket implanted nanoscale n-MOSFET," Journal of Electron Devices, ISSN 1682-3427, vol. 8, pp 263-267, October 2010.
[12] M. H. Bhuyan, F. Ferdous and Q. D. M. Khosru, "A threshold voltage model for sub-100 nm pocket implanted NMOSFET," Proceedings of the 4th IEEE International Conference on Electrical and Computer Engineering, Dhaka, Bangladesh, 19-21 December 2006, pp. 522-525.
[13] X. Zhou, K. Y. Lim and D. Lim, "Physics-Based threshold voltage modeling with Reverse Short Channel Effect," Journal of Modeling and Simulation of Microsystems, Vol. 2, No. 1, pp. 51-56, 1999.
[14] X. Zhou, K. Y. Lim and D. Lim, "A general approach to compact threshold voltage formulation based on 2-D numerical simulation and experimental correlation for deep-submicron ULSI technology development," IEEE Trans. on Electron Devices, vol. 47, no. 1, pp. 214-221, Jan. 2000.
[15] A. Mondal, A. Roy, R. Mitra and A. Kundu, "Comparative Study of Variations in Gate Oxide Material of a Novel Underlap DG MOS-HEMT for Analog/RF and High Power Applications," Silicon, Springer, vol. 12, pp. 2251–2257, 2020.
[16] A. A. Sayem, Y. Arafat and M. M. Rahman, "Effect of High k-Dielectric as Gate Oxide on Short Channel Effects of Junction-less Transistor," Proceedings of the 2nd IEEE International Conference on Advances in Electrical Engineering (ICAEE 2013), 19-21 December 2013, Dhaka, Bangladesh, pp. 115-118.
[17] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," Journal of Materials Science and Engineering R, vol. 88, 2015, pp. 1-41.
[18] G. Sethi, M. Olszta, J. Li, J. Sloppy, M. W. Horn, E. C. Dickey and M. T. Lanagan, "Structure and dielectric properties of amorphous tantalum pentoxide thin film capacitors," 2007 Annual Report Conference on Electrical Insulation and Dielectric Phenomena, pp. 815-818.
[19] K. Koley, A. Dutta, B. Syamal, S. K. Saha, C. K. Sarkar, "Subthreshold analog/RF performance enhancement of underlap DG FETs with high- k spacer for low power applications," IEEE Transaction on Electron Devices, vol. 60, no. 1, pp, 63-69, 2013.
[20] M. H. Bhuyan and Q. D. M. Khosru, "Linear Profile Based Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET," Journal of Electron Devices, France, 1682-3427, vol. 7, April 2010, pp 235-240.
[21] M. H. Bhuyan and Q. D. M. Khosru, "Linear Pocket Profile Based Pinch Off Voltage Model for Nanoscale n-MOSFET," Proceedings of the 2nd IEEE International Conference on Electrical, Computer and Telecommunication Engineering (ICECTE 2016), Rajshahi University of Engineering and Technology (RUET), Rajshahi, Bangladesh**,** 8-10 December 2016, pp. 1-4, *doi: 10.1109/ICECTE.2016.7879624***.**
[22] M. H. Bhuyan and Q. D. M. Khosru, "Inversion Layer Effective Mobility Model for Pocket Implanted Nano Scale n-MOSFET," International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, ISSN: p:2010-376X, e:2010-3778, vol. 5, no. 1, 2011, pp. 1-8.
[23] M. H. Bhuyan and Q. D. M. Khosru, "Analytical Subthreshold Drain Current Model Incorporating Inversion Layer Effective Mobility Model for Pocket Implanted Nano Scale n-MOSFET," International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, ISSN: p: 2010-376X, e: 2010-3778 vol. 7, no. 4, 2013, pp. 465 - 472.

Muhibul Haque Bhuyan (MIEEE'07–) became a Member (M) of World Academy of Science, Engineering and Technology in 2005, born in Dhaka, Bangladesh on 25 July. He did his BSc, MSc, and PhD degrees in Electrical and Electronic Engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 1998, 2002, and 2011 respectively.

Currently, he is working as a Professor of the Department of Electrical and Electronic Engineering of Southeast University, Dhaka, Bangladesh. He led this department as the Departmental Chairman from 1st March 2016 to 10 March 2021. Previously, he worked at the Green University of Bangladesh, Dhaka as a Professor and Chairman of the EEE Department; Daffodil International University, Dhaka, Bangladesh as an Assistant Professor and Head of ETE Department; Presidency University, Dhaka, Bangladesh as an Assistant Professor and American International University Bangladesh (AIUB), Dhaka as a Faculty Member since June 1999. He also worked as a Researcher in the Center of Excellence Program of Hiroshima University, Japan from July 2003 to March 2004. So far, he has published over 40 research papers in national and international journals and presented over 50 research works at national and international conferences. His research interests include MOS device modeling, biomedical engineering, control system design, outcome-based engineering education, assessment, and evaluation.

Prof. Bhuyan is a Member of IEEE, USA, Executive Member of Bangladesh Electronics and Informatics Society (BEIS), and Fellow of the Institution of Engineers Bangladesh (IEB). He is a regular reviewer and technical/editorial/organizing committee member of several national and international journals and conferences. He was the Organizing Chair of the recently held IEEE 22nd International Conference on Computer and Information Technology (ICCIT) in Dhaka, Bangladesh during 18-20 December 2019. He is the recipient of the Bangladesh Education Leadership Awards (Best Professor in Electrical Engineering) in 2017 from the South Asian Partnership Awards, Mumbai, India.